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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	P4158/PSM
First Inventor or Application Identifier	Massimo Sutera
Title	see "Other" section #15
Express Mail Label No.	EM104247475US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 14]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]
4. Oath or Declaration [Total Pages 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: title: "Method for reducing noise in integrated circuit layouts"

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
    Prior application information: Examiner _____ *Group / Art Unit:* _____

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17. CORRESPONDENCE ADDRESS

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JC600 U.S. PTO 10/29/99

JC564 U.S. PTO 09/430350 10/29/99

This application is submitted in the name of inventors Massimo Sutera and Alan Smith, assignors to Sun Microsystems, Inc.

SPECIFICATION

METHOD FOR REDUCING NOISE IN INTEGRATED CIRCUIT LAYOUTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates noise problems in integrated circuits. More particularly, the present invention provides a method for inserting buffers into an integrated circuit layout during the place and route stage in order to reduce the overall noise introduced into conductive paths in a given design.

2. The Background Art

As the speed of signals within integrated circuits increases and the distance between conductive paths decreases, the problem of reducing the susceptibility of conductive paths to noise becomes increasingly important.

In the prior art conversion process between design and layout for integrated circuit systems, there are four major steps which are accomplished by system designers. Those four major steps include place and route of the standard cell design, physical design verification to ensure consistency between the layout and the schematic, parisitic extraction of the interconnect, and analysis of the extracted data to generate a noise analysis report.

When correcting the physical circuit layout in a prior art conversion process, a designer typically must either manually move wires and circuits in order to minimize or eliminate those noise problems, or may instead increase the size of the driver supplying signals to a conductive path which is deemed to be noise sensitive.

This manual process is extremely time–consuming and very tedious because by moving conductive paths or increasing drivers is likely to cause new noise problems. Those new noise problems must then be corrected, potentially causing yet a third set of noise problems. Thus, manually correcting a circuit layout in order to solve noise problems often requires considerable effort and several very time–consuming iterations.

It would therefore be beneficial to provide a method for automatically determining potentially noisy areas within circuit layouts at the place and route stage, and for correcting problems related to areas of specific concern.

SUMMARY OF THE INVENTION

A method for minimizing noise in an integrated circuit is described, the method including choosing a net to be analyzed, determining that the total path length of conductive paths coupled to a driver within the net exceeds a maximum acceptable length for that driver according to the minimum acceptable noise levels for that given net, and inserting at least one buffer within the net at a position

which is within the maximum acceptable length for conductive paths coupled to the driver.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a prior art physical circuit layout having potential noise problems.

FIG. 2 shows a prior art curve of noise amplitude vs. conductive path length.

FIG. 3 is a flowchart depicting a method of the present invention.

FIG. 4 shows the example of FIG. 1 after having placed buffers according to a method of the present invention.

DETAILED DESCRIPTION OF ONE EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons who are familiar with this disclosure.

The present invention provides a method for correcting potentially noisy circuit layouts at the place and route stage during the process of converting an electronic design into a physical circuit layout.

FIG. 1 is a block diagram of a prior art physical circuit layout having potential noise problems.

Referring to FIG. 1, layout 10 includes driver/receivers 12 and 14 coupled together using conductive path 16. Further included are driver/receivers 18 and 20, driver 22 and receiver 24. Driver/receiver 18 is coupled to driver/receiver 20 using conductive path segments 26 and 28. At the intersection of conductive path segments 26 and 28, a conductive path segment 30 is coupled thereto. Driver 22 and receiver 24 are coupled to conductive path segments 32 and 34 respectively. Conductive path segments 32 and 34 are further coupled to conductive path segment 30.

The present invention analyzes each net individually to determine whether a given net is likely to have more than an acceptable level of noise coupled to it from external sources. External sources are considered to be anything other than net components such as driver/receiver combinations or drivers or receivers individually.

Although the coupling capacitance between interconnects is a source of potential coupling noise problems, the symptom of the noise peak is demonstrated

at the output of the receiving cell. Different CMOS cells have differing tolerance for coupling noise impinging on their inputs. The choice for the maximum allowable wire length for noice violations to be prevented is therefore not only dependant on the strength of the victim and aggressor drivers, but also on the type of cell at the end of the victim interconnect.

The present invention noise analysis is performed using well–known curves for various driver circuits of noise amplitude vs. the length of a conductive path coupled to that driver circuit. It is well–known that a conductive path of a given length being driven by a weak driver will have a higher susceptibility to noise than that same conductive path when driven by a stronger driver.

For each conductive path, there is a given amount of noise that can be tolerated, depending on what signals on that conductive path are accomplishing. It is up to the circuit designer to determine what the acceptable levels of noise will be on the various types of conductive paths being used in a given design. Such an acceptable level might be pictorially represented as line 40 in FIG. 2. The point at which line 40 intersects with a driver noise amplitude line determines the maximum length of conductive path that may be between a driver in the receiver without any intervening circuitry such as buffers or other circuits.

FIG. 3 is a flowchart depicting a method of the present invention.

Referring to FIG. 3, the method begins at block 50 where a net is chosen for analysis. It is contemplated that all critical nets in a given design will be analyzed. However, not all nets in every design will necessarily be analyzed according to the present invention.

At block 52, using the noisy amplitude vs. distance data which is known by those of ordinary skill in the art and the acceptable noise levels previously determined for that given circuit type, it is determined whether the net chosen at block 50 is likely to exceed the acceptable noise levels. That question is posed a block 54, and if the chosen net is likely to exceed maximum acceptable noise levels, it is determined, at block 56, whether a larger driver is available in the driver library which would solve the problem. If so, the method proceeds at block 58 where a larger driver is chosen to replace the previously determined weaker driver, thus solving the noise problem for this net.

An example of a larger driver solving the problem is seen in FIG. 2 where, in this example, the driver having the characteristics shown by curve 58 might have been originally chosen for the physical layout. Suppose in this example, point 60 on curve 58 represents the length of the conductive path being analyzed. It is easily seen that point 60 is above the acceptable noise level line 40. However, curves 62 and 64, representing stronger drivers, for the same length of conductive path would result in acceptable noise levels as represented by points 66 and 68 respectively.

If, at step 56, a larger driver was not available, the method proceeds at block 70 where a buffer is placed at a location which would increase signal levels on the net. Locations where drivers are placed may be thought to be locations where the previous net ends and a new net begins. Thus, a buffer is placed at a location which would cause the conductive path between the driver and the buffer to be shorter than would otherwise have occurred. Since the conductive path is shorter, there is less susceptibility to noise.

In order to properly place a buffer so as to minimize the noise in a given net, it is necessary to know the point at which acceptable noise level line 40 and FIG. 2 crosses the curve for the given driver. Thus, if a driver is employed which is represented by curve 62, it is necessary to know where point 72 is located. Knowing where point 72 is located gives you the maximum length of conductive path allowed in order to achieve an acceptable noise level for that conductive path.

When determining where to place a buffer, it is important to recognize that a conductive path includes all conductive path segments leaving a given driver, including all intersecting paths. Using the example of FIG. 1, the total length of conductive path segments between driver/receiver 18 and point 72 on conductive path segment 30 includes all of conductive path segment 26, all of conductive path segment 28, and that portion of conductive path 30 between point 72 and intersection point 74.

FIG. 4 shows the example of FIG. 1 after having placed buffers according to the method of the present invention.

Referring to FIG. 4, the net which includes driver/receiver 12, driver/receiver 14, and conductive path 16 has not been duplicated because it was previously determined that this net resulted in acceptable noise levels. The remaining net includes driver/receiver 18 and receiver 24 from FIG. 1, new driver/receiver 80, and new driver 82.

Assume now that it is time to analyze driver/receiver 18 and the conductive paths coupled thereto. Using the curve associated with driver/receiver 18, a given maximum length for conductive paths coupled to driver/receiver 18 will be known because the maximum acceptable length for those conductive paths will have been determined by knowing the maximum acceptable noise level allowed on those conductive paths.

Assume that the various lengths of conductive path segments 84, 86, 88, and 90 add up to the maximum acceptable length for a conductive path coupled to driver/receiver 18. It is acceptable then, to provide a buffer at any point on conductive paths 84, 86, 88, or 90.

It is most desirable at this point, to determine if there are timing issues with respect to driver/receiver 18 and/or driver/receiver 80 which would make it more desirable to place a buffer in either conductive path segment 84 or either of conductive path segments 88 or 90. If it is critical that signals being transmitted

from driver/receiver 80 travel more quickly over the various conductive paths to, for example, receiver 24, it would be more beneficial to place a required buffer within conductive path 84, rather than, for example, within conductive path 86.

Now assume that buffer 92 has been placed within conductive path 84 because it is necessary that signals from driver/receiver 80 arrive at receiver 24 as quickly as possible. Once buffer 92 has been placed, the new question becomes whether the total conductive path length between the output of driver 92 and the input to receiver 24 meets the previously defined criteria for noise.

If the previously defined criteria for noise is not met by the remaining total conductive path length, is again necessary, at block 96 of FIG. 3, to determine where to place another buffer. Now, the FIG. 2 curve to be used is that curve associated with buffer 92. A new maximum acceptable path length will be determined from that curve, and it may be necessary to add a second buffer such as buffer 96.

Those of ordinary skill in the art having the benefit of this disclosure would readily recognize that the methods described herein may easily be incorporated in place and route software. It is also contemplated that the methods described herein may be incorporated into a state machine or other application–specific integrated circuits.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is Claimed is:

1. A method for minimizing noise in an integrated circuit comprising:

choosing a net to be analyzed;

determining that the total path length of conductive paths coupled to a driver within said net exceed a maximum acceptable length for that given driver according to the minimum acceptable noise levels for that given net; and

inserting at least one buffer within said net at a position which is within the maximum acceptable length for conductive paths coupled to said driver.

2. A machine readable medium having machine instructions stored thereon, the machine readable instructions including a method for minimizing noise in an integrated circuit, the method comprising:

choosing a net to be analyzed;

determining that the total path length of conductive paths coupled to a driver within said net exceed a maximum acceptable length for that given driver according to the minimum acceptable noise levels for that given net; and

inserting at least one buffer within said net at a position which is within the maximum acceptable length for conductive paths coupled to said driver.

2. A method for minimizing noise in an integrated circuit comprising:

choosing a net to be analyzed;

determining that the total path length of conductive paths coupled to a first driver within said net exceed a maximum acceptable length for said first driver according to the minimum acceptable noise levels for said net;

determining that a second driver exists which provides a stronger signal output then said first driver and which also is available to replace said first driver;

replacing said first driver with said second driver;

determining, once said first driver is replaced, that the total path length of conductive paths coupled to said second driver within said net exceed a maximum acceptable length for said second driver according to the minimum acceptable noise levels for said net;

inserting at least one buffer within said net at a position which is within the maximum acceptable length for conductive paths coupled to said driver.

4. A machine readable medium having machine instructions stored thereon, the machine readable instructions including a method for minimizing noise in an integrated circuit, the method comprising:

choosing a net to be analyzed;

determining that the total path length of conductive paths coupled to a first driver within said net exceed a maximum acceptable length for said first driver according to the minimum acceptable noise levels for said net;

determining that a second driver exists which provides a stronger signal output then said first driver and which also is available to replace said first driver;

replacing said first driver with said second driver;

determining, once said first driver is replaced, that the total path length of conductive paths coupled to said second driver within said net exceed a maximum acceptable length for said second driver according to the minimum acceptable noise levels for said net;

inserting at least one buffer within said net at a position which is within the maximum acceptable length for conductive paths coupled to said driver.

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ABSTRACT OF THE DISCLOSURE

A method for minimizing noise in an integrated circuit is described, the method including choosing a net to be analyzed, determining that the total path length of conductive paths coupled to a driver within the net exceed a maximum acceptable length for that given driver according to the minimum acceptable noise levels for that given net, and inserting at least one buffer within the net at a position which is within the maximum acceptable length for conductive paths coupled to the driver.

FIG. 1
Prior Art

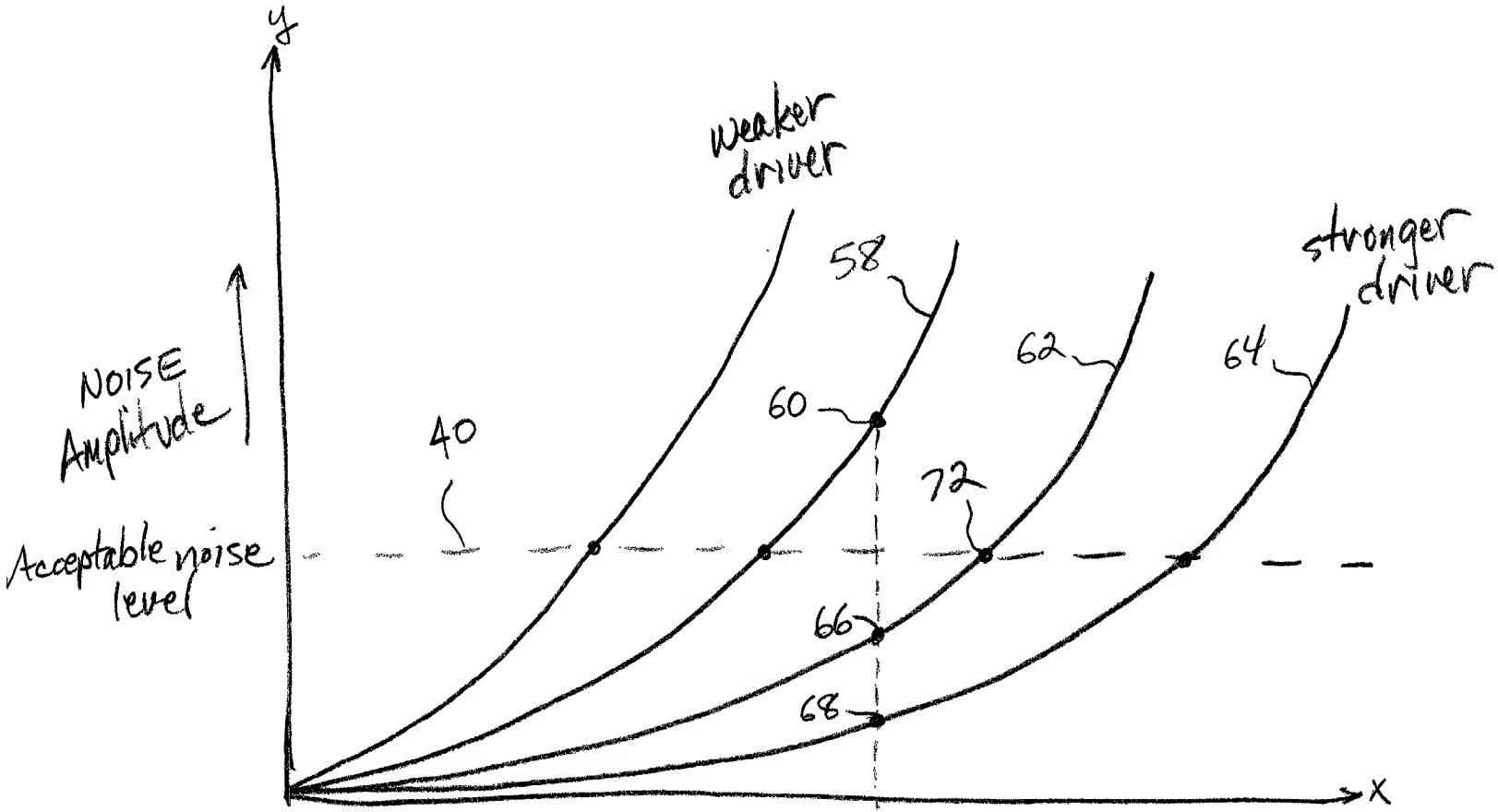
y
weaker driver
stronger driver
58
62
64
60
40
72
NOISE Amplitude
Acceptable noise level
66
68
x
Length of conductive path

FIG. 2

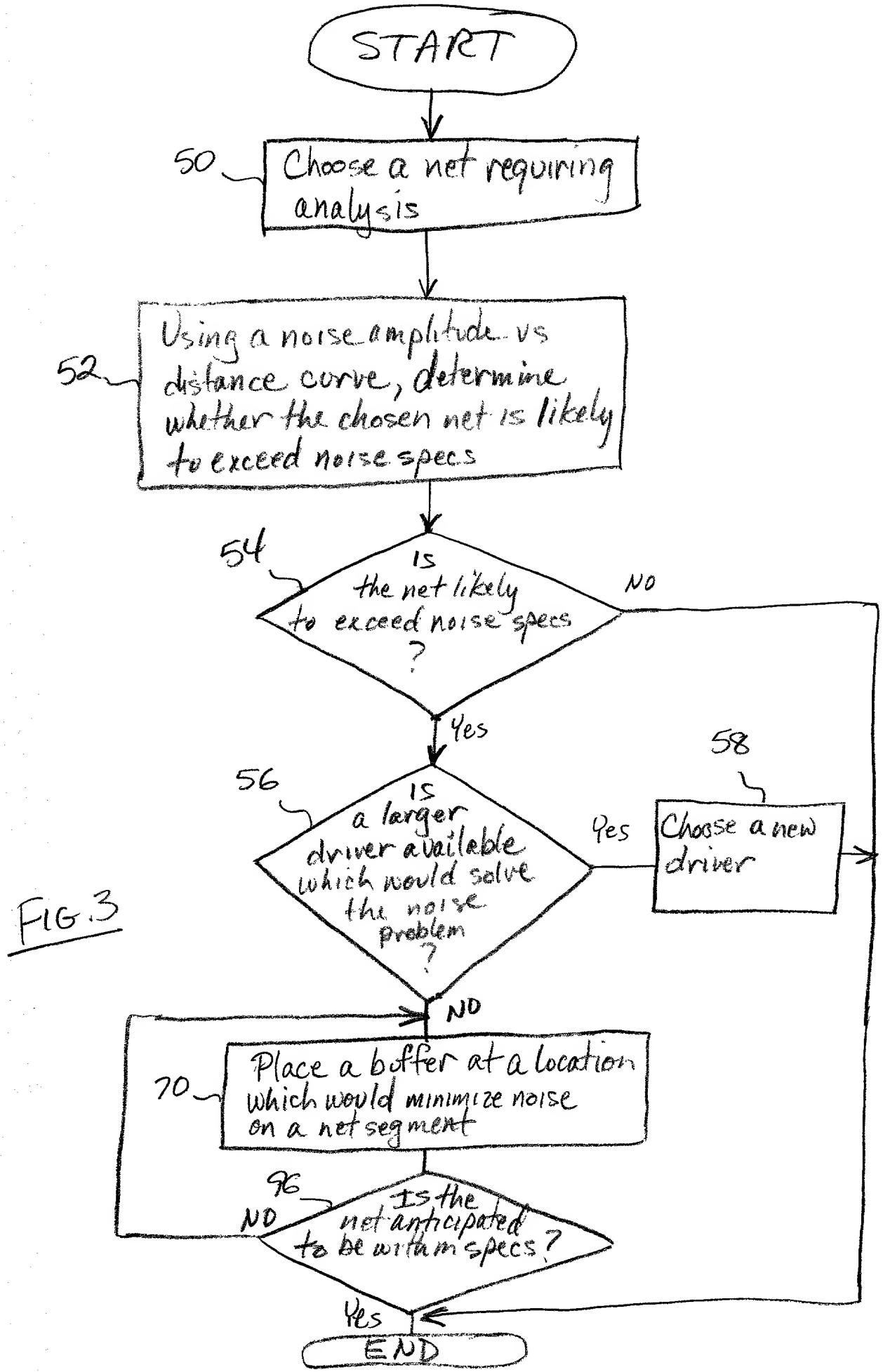
START
50
Choose a net requiring analysis
52
Using a noise amplitude vs distance curve, determine whether the chosen net is likely to exceed noise specs
54
Is the net likely to exceed noise specs ?
NO
Yes
56
Is a larger driver available which would solve the noise problem ?
Yes
58
Choose a new driver
NO
70
Place a buffer at a location which would minimize noise on a net segment
96
Is the net anticipated to be within specs ?
NO
Yes
END

FIG. 3

Receiver
80
90
88
41
44
86
92
81
Driver
96
Receiver
34
32
Receiver
24
82

FIG. 4

DECLARATION

As a below-named inventor, I hereby declare that:

My correct residence, post office address and citizenship are stated below next to my name.

I believe myself to be the original, first and sole inventor (if only one name is listed below) or an original and first joint inventor (if more than one name is listed below) of the subject matter which is disclosed and claimed and for which a patent is sought on the invention entitled:

METHOD FOR REDUCING NOISE IN INTEGRATED CIRCUIT LAYOUTS

The specification of this subject matter:

X is attached hereto.

☐ was filed on xxxxx, 199x;

was assigned serial No. xxxxxx;

which was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified patent application, including the claims, as amended by any amendment(s) referred to above. I believe the subject matter claimed in the above-identified application to be new and to be unobvious to persons of ordinary skill in the art in view of the prior art of which I am aware. I further hereby state that the specification of the above identified patent application adequately describes how to make and use the claimed invention, and further that it sets forth the best mode for practicing the invention known to me as of the date that the application was filed. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. §1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Application No.	Country	Filing Date	Priority Claimed

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in these prior United States application(s) in the manner provided by 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

Application No.	Filing Date	Status (Issued, Pending, Abandoned)

FULL NAME OF FIRST Name MIDDLE Initial(s) LAST Name

INVENTOR 1

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I further declare that all statements made herein of my own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Date: 10/14/99	Signature of Inventor 2	Date: 10/14/99